REMARKS

No claims are amended. Reconsideration and allowance of the pending claims is requested in light of the following remarks.

Claim Rejections – 35 USC § 112

Claims 5-7 and 9-17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The applicants disagree.

As a preliminary matter, it now well accepted that a satisfactory description may be in the claims or ***any other portion of the originally filed specification***. MPEP 2163(I), emphasis added. Possession may be shown ***in a variety of ways*** including description of an actual reduction to practice, ***or*** by showing that the invention was "ready for patenting" ***such as by the disclosure of drawings . . ., or*** by describing distinguishing identifying characteristics. Id., emphasis added. An applicant may show possession of an invention by ***disclosure of drawings*** (see MPEP 2163(II)(A)(3)(a); emphasis added).

With regard to claim 5, it is alleged that there is no support in the specification for a line width of the first surface region being equal to a line width of the impurity implantation region.

To the contrary, the feature of an impurity implantation region is fully supported by the originally filed specification (see, e.g., page 7, line 27 and FIG. 5a; page 9, line 12 and FIG. 6a; page 10, line 4 and FIG. 7a.).

Claim 5 recites that the impurity implantation region includes a first surface of the semiconductor substrate. This feature is fully supported by the originally filed specification, see, e.g., FIGs. 5a, 6a, and 7a, where the impurity implantation regions are illustrated as including a surface of the semiconductor substrate.

Furthermore, the term "line width" is fully supported by the originally filed specification. See, e.g., page 5, lines 23-24; FIG. 3; FIG. 4; FIGs. 5a and 5b; FIGs. 6a and 6b; FIGs. 7a and 7b.

Thus, each element of the feature identified by the Examiner is supported by the specification. Futhermore, FIGs. 5a, 6a, and 7a all illustrate that the line width of the

impurity implantation region is equal to the line width of the first surface region of the semiconductor substrate that is included in the impurity implantation region.

Finally, MPEP 2163.04 states that the ***Examiner has the initial burden*** of presenting ***by a preponderance of evidence*** why a person skilled in the art would not recognize in the ***applicant's disclosure*** a description of the invention defined by the claims (emphasis added). Given that support for this feature of claim 5 ***does exist*** in the specification, this burden has not been met.

With regard to claims 10 and 14, it is alleged that "[t]here is no support in the specification for a device comprising a first sector not reaching either one of the source region and the drain region, wherein the impurity implantation region occupies the entire top surface of the substrate, as recited in claims 10 and 14."

Claims 10 and 14 both recite "a first sector not reaching either one of the source region and the drain region." Contrary to allegations, support for this feature exists in the original specification where it states "the first sector does not reach either one of the source and drain regions" (page 7, lines 22-23).

Given that support for the above feature of claims 10 and 14 ***does exist*** in the original specification, the Examiner has not fulfilled the initial burden of presenting, by a preponderance of evidence, why a person skilled in the art would not recognize in the applicant's disclosure a description of the invention defined by the claims. MPEP 2163.04, emphasis added.

As to the other disputed feature regarding the impurity implantation region, the Examiner has ignored additional relevant portions of claim 10 and 14. As recited in claim 10, the feature reads "the impurity implantation region further comprising ***a first surface region*** that functions as a depletion channel and that occupies the entire top surface of the semiconductor substrate ***within the lateral extent of the impurity implantation region***" (claim 10, emphasis added). As recited in claim 10, the feature reads "the impurity implantation region further comprising ***a first surface region*** that functions as a depletion channel and that occupies the entire top surface of the semiconductor substrate ***within the first sector***" (claim 14, emphasis added).

Thus, the disputed feature describes the first surface region of the impurity implantation region. The first surface region occupies the entire top surface of the semiconductor substrate ***within*** the lateral extent of the impurity implantation region (claim 10) or ***within*** the first sector (claim 14). These features are fully supported at, e.g., FIG. 7a.

Given that support for the above feature of claims 10 and 14 ***does exist*** in the original specification, the Examiner has not fulfilled the initial burden of presenting, by a preponderance of evidence, why a person skilled in the art would not recognize in the applicant's disclosure a description of the invention defined by the claims. MPEP 2163.04, emphasis added.

Regarding claim 18, the Examiner is correct that there is no support on page 11, lines 3-5 of the specification for the recited open drain and enhancement transistors, the gate of the enhancement transistor having a length greater than the length of the gate of the open transistor. It appears that the applicants mistakenly referenced a working copy of the application that was different from the application as filed. Support for these features may be found in the application as filed at, e.g., page 2, lines 4-10 (referring to FIG. 1); page 2, lines 16-24 (referring to FIG. 2); page 2, lines 25-28 (referring to FIGs. 3 and 4); page 3, lines 24-26); page 6, lines 24-28 (referring to FIGs. 5a and 5b); page 7, lines 12-16 (referring to FIGs. 6a and 6b); page 7, lines 21-25 (referring to FIGs. 7a and 7b).

For the above reasons, the applicants submit that the rejections under 35 USC § 112, first paragraph, are overcome.

Claims 5-9, 11 and 15 are also rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The applicants disagree.

In particular, it is alleged that it is unclear as to what distances are represented by the line widths of the first surface, the impurity implantation region and the first sector. Although there is no line in the figures like those labeled F and W3 that describe the line widths of the active regions and the gates, respectively, such lines are not required.

During patent examination, the pending claims must be given "the broadest reasonable interpretation ***consistent with the specification***." MPEP 2111, *citing* In re Prater, 415 F.2d 1393, 1404-05 (CCPA 1969); emphasis added. The line widths F and W3 refer to the widest part of the active regions and the gates, respectively. In order to be consistent with the specification, "line widths" as applied to the first surface, the impurity implantation region, and the first sector must be given the same meaning.

For the above reasons, the applicants submit that the rejections under 35 USC § 112, second paragraph, are overcome.

Claim Rejections – 35 USC § 103

Claims 5-7 and 9-17, insofar as they are in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,668,021 to Subramanian et al. ("Subramanian") in view of Applicant Admitted Prior Art ("AAPA"). The applicants disagree.

Claims 5, 10, and 14 all recite a semiconductor substrate of a first conductivity type. Both Subramanian and AAPA teach this. Claims 5, 10 and 14 also recite an impurity implantation region having impurities of a second conductivity type. Subramanian teaches an impurity implantation region 24 of a second conductivity type (FIG. 6; column 3, lines 56-61). AAPA teaches an impurity implantation region 46 of a first conductivity type and an impurity implantation region 44 of a second conductivity type (FIG. 3).

The applicants agree that Subramanian does not teach the feature recited in claim 5 that "a line width of the first surface region is equal to a line width of the impurity implantation region." However, AAPA is alleged to teach this feature. The applicants disagree at this point.

It must be remembered that the impurity implantation region of a second conductivity type taught by AAPA is region 44, ***not*** region 46 (FIGs. 2 and 3; page 2, lines 16-33; emphasis added). It is evident from FIG. 2 that AAPA's region 44 does not have a first surface region with a line width that is equal to a line width of the region 44. Rather, the surface region of impurity implantation region 44 has a line width smaller than that of the impurity implantation region 44.

Similar to claim 5, claim 10 recites that the impurity implantation region includes a first surface region that occupies the entire top surface of the semiconductor substrate within the lateral extent of the impurity implantation region. Thus, for the same reason discussed above with respect to claim 5, AAPA does not teach or suggest this feature.

Similar to claims 5 and 10, claim 14 recites that the impurity implantation region includes a first surface region that occupies the entire top surface of the semiconductor substrate within the first sector. Thus, for the same reason discussed above with respect to claims 5 and 10, AAPA does not teach or suggest this feature.

Consequently, the Subramanian/AAPA combination does not establish a *prima facie* case of obviousness for claims 5, 10, 14 because it does not teach or suggest the feature of an impurity implantation region of a second conductivity type that includes a first surface region, the line width of the first surface region equal to a line width of the impurity implantation region (MPEP 2143.03).

In addition to failing to teach or suggest all features of claims 5, 10, and 14, the Subramanian/AAPA combination also fails to establish *prima facie* obviousness because there is no suggestion or motivation to modify Subramanian using AAPA in the manner that the Examiner suggests. MPEP 2143. In other words, there is no suggestion or motivation to combine AAPA with Subramanian to achieve the feature of an impurity implantation region of a second conductivity type that includes a first surface region, the line width of the first surface region equal to a line width of the impurity implantation region.

First, as mentioned above, AAPA teaches a semiconductor region 30 of a first conductivity type, an impurity implantation region 46 of a first conductivity type, and an impurity implantation region 44 of a second conductivity type (FIG. 3). Subramanian teaches a semiconductor substrate 10 of a first conductivity type and an impurity implantation region 24 of a second conductivity type (FIG. 6; column 3, lines 56-61). The Examiner has suggested that it would be obvious to modify Subramanian's impurity implantation region 24 (having a second conductivity type) to have the shape of AAPA's impurity implantation region 46 (having a first conductivity type).

To the contrary, AAPA teaches away from modifying Subramanian in such a manner because AAPA region 46 is of the opposite conductivity type to Subramanian's region 24. Furthermore, the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. MPEP 2143.01, *citing* In re Mills, 916, F.2d 680 (Fed. Cir. 1990). The shape of AAPA region 46 in no way suggests the desirability of modifying Subramanian's buried junction region 24 to have the same or similar shape.

Secondly, modifying Subramanian with AAPA in the manner that Examiner suggests would render Subramanian unsuitable for its intended purpose. Subramanian's stated purpose is to fabricate a channel region that contains both surface channel regions and a buried junction region, thus obtaining a device that utilizes the advantages of both the surface channel region and the buried junction region (column 2, lines 8-13).

Subramanian states that "buried channel devices" have a "buried junction region" within the channel region (column 1, lines 31-32). Subramanian's region 24 is a buried junction region (column 3, lines 36-39). According to S. Wolf in Silicon Processing for the VLSI Era, Vol. III, pgs. 292-293 (attached in Appendix), unlike the case for conventional surface-channel devices, in buried channel devices more current flows in a channel ***beneath the surface*** of the device than at the surface (emphasis in original). This is entirely in keeping with Subramanian's statement that the peak dopant concentration of buried junction

region 24 is placed just ***below the surface*** of the semiconductor substrate (column 3, lines 65-67; emphasis added).

Based on the above, it is undisputable that the peak current flow in Subramanian's buried junction region 24 does not take place at the surface of the semiconductor substrate. To the contrary, it can be seen by the shape of AAPA's region 46 that the maximum current flow will occur at the surface of the device, because that is where the most impurities are located.

Since modifying Subramanian's buried channel region 24 to have the shape of AAPA region 46 would cause region 24 to be unsatisfactory for its intended purpose as a buried junction region, there is no suggestion or motivation to make the proposed modification. MPEP 2143.01, *citing* In re Gordon, 733 F.2d 900 (Fed. Cir. 1984).

Thirdly, for the same reason as discussed above, modifying Subramanian's buried junction region 24 to have the shape of AAPA region 46 would cause the buried junction region 24 to become a surface channel region. This is contrary to the principle of operation of Subramanian, who states that MOS devices fabricated in accordance with his invention contain both surface channel regions and a buried channel region (column 2, lines 8-13). Consequently, the teachings of Subramanian/AAPA are not sufficient to render the claims *prima facie* obvious. MPEP 2143.01, *citing* In re Ratti, 270 F.2d 810 (CCPA 1959).

Fourthly, the Examiner has consistently (and improperly) used portions of applicants' disclosure that are critical of AAPA to find a suggestion or motivation to combine AAPA with Subramanian.

For example, the motivation, as stated in the last office action, "in order to use the device in an application which requires a pull-up transistor" is taken from the applicants' statement that "[t]he invention provides an improved pull-up transistor that is to be used in place of the enhancement transistor B of the prior art" (Summary of the Invention). The teaching or suggestion to make the claimed combination must be found in the prior art, not in the applicant's disclosure. MPEP 2143, *citing* In re Vaeck, 947 F.2d 488 (Fed. Cir. 1991).

The other stated motivation to combine AAPA and Subramanian, that of "in order to adjust the characteristics of the device according to the requirements of the application in hand," is so generic as to be worthless. The level of skill in the prior art cannot be relied upon to provide the suggestion to combine references. MPEP 2143.01, *citing* Al-Site Corp. v. VSI Int'l Inc., 174 F.3d 1308 (Fed. Cir. 1999). It was alleged that it would be obvious to modify Subramanian's buried junction region 24 by making it the same or similar shape to AAPA region 46. It has yet to be shown that AAPA provides any objective reason for

making such a modification to Subramanian, without such an objective reason there can be no *prima facie* case of obviousness. See, e.g., MPEP 2143.01, *citing* Ex parte Levengood, 18 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993). As explained above, considering the fact that Subramanian requires the region 24 to be a buried junction region having the associated characteristics of such a region, there is no objective reason to modify it into a surface channel region as taught by AAPA region 46. Further considering the fact that region 46 is of a different conductivity type than Subramanian region 24, such a modification is even more implausible.

For any of the above reasons, the applicants believe that the 35 USC § 103 rejections to claims 5, 10, and 14 are overcome. The remainder of claims 5-7 and 9-17 depend from claims 5, 10, or 14. Any claim that depends from a nonobvious independent claim is also nonobvious. MPEP 2143.03, *citing* In re Fine, 837 F.2d 1071 (Fed. Cir. 1988).

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of U.S. Patent No. 6,184,559 to Hayakawa et al. ("Hayakawa"). The applicants disagree.

Claim 18 recites that both the open drain transistor and the enhancement transistor each have a gate, a source region, a drain region, and a channel region defined between the source region and the gate region. Claim 18 also recites that the gate of the enhancement transistor is longer than the gate of the open-drain transistor.

Hayakawa FIG. 1 teaches a single source region 101 (column 3, line 65), a single drain region 102 (column 3, line 66), and a multi-gate electrode structure where the gate electrodes 103, 104, and 105 are electrically connected (column 3, lines 60-61; column 4, lines 5). Although there are three gate electrodes 103, 104, 105, electrically it is the same gate. Thus, Hayakawa FIG. 1 shows only a single thin-film transistor having one drain region and one source region (column 3, lines 21-25). The relative lengths A, B, C, of Hayakawa's gate electrodes 103, 104, 105, respectively, do not teach or suggest that the gate of the enhancement transistor taught by AAPA should be longer than the gate of the other, open-drain transistor taught by AAPA. At most, Hayakawa teaches that a gate of each of the individual transistors could have the shape shown in FIG. 1.

Consequently, a *prima facie* case is not established for claim 18 because the AAPA/Hayakawa combination fails to teach or suggest every feature of the claim. MPEP 2143.03.

Claims 19-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Hayakawa as applied to claim 18 above, and further in view of Subramanian. The

applicants disagree. Claims 19-26 depend from claim 18. Any claim that depends from a nonobvious independent claim is also nonobvious. MPEP 2143.03, *citing* In re Fine, 837 F.2d 1071 (Fed. Cir. 1988).

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 5-7 and 9-26 of the application as amended is requested. Please telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Date: June 24, 2004

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in surface-channel NMOSFETs: (1) a *pn* junction is formed beneath the gate oxide in the channel, extending to a depth Y_j (as can also be seen in Fig. 5-54); and (2) the potential minimum is moved away from the surface. The latter effect gives rise to important device-behavior effects that differ from those of surface-channel MOSFETs. We explain this behavior by first comparing the location of the potential minimum in such boron-implanted-layer PMOSFETs to its location in surface-channel MOSFETs.

Figure 5-55 shows the one-dimensional potential diagrams of two PMOS devices, one with a p^+-polysilicon gate and a uniformly doped *n*-substrate (3.4×10^{16} cm^{-3}), and the other with a n^+-polysilicon gate and a shallow boron V_T-adjust implant. In both devices $V_{GS} = 0V$, and $V_{DS} = -5V$. The potential profile is taken at the point along the channel at which the longitudinal field vanishes (to match the fact that in a MOS-C there is also no longitudinal electric field). In the p^+-poly gate device the potential minimum is located at the surface, implying that such a device will operate much like the surface-channel NMOSFETs described in chap. 4. In the PMOS structure with the n^+-poly gate and boron V_T-adjust implant, however, we see that the potential minimum is away from the Si surface. The mobile carriers (holes) will thus be found at highest density near the location of the potential minimum. This implies that, unlike in the

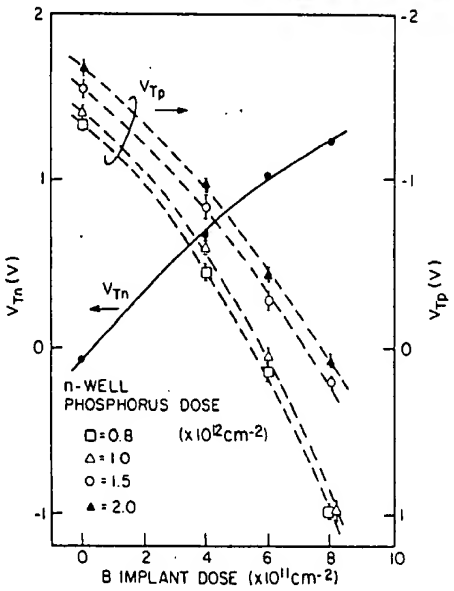

Fig. 5-53 Threshold voltages of *n*-channel (V_{Tn}) and *p*-channel (V_{Tp}) transistors as a function of boron threshold-adjustment dose. The CMOS structure uses an *n*-well implanted into a *p*-substrate (whose doping level is 6×10^{14} atoms/cm^3). V_{Tp} results are shown for various implant doses of the *n*-well.[71] (© 1980 IEEE).

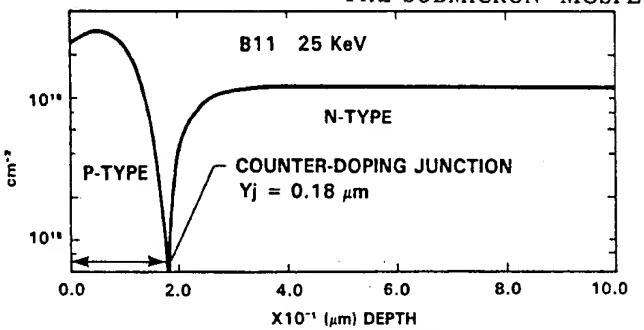

Fig. 5-54 Simulated channel profile for a *p*-channel MOSFET with an implanted B dose at the channel surface.[115] (© 1984 IEEE).

case of conventional surface-channel devices, more current will flow in a channel *beneath* the surface of the device than at the surface.[72] Such PMOS devices are therefore referred to as *buried-channel* (BC) transistors. As also seen in Fig. 5-56 (which gives the calculated variation of the potential as a function of distance below the surface as the channel *pn* junction depth is varied), the potential minimum moves further into the substrate as the thickness of the implanted *p*-layer is increased. The mobility of carriers in the buried channel is ~15% higher than carriers at the surface, and thus BC MOSFETs exhibit a somewhat larger drive current than comparable surface channel FETs. While this is an advantage, it is outweighed by several other disadvantages exhibited by BC FETs. Let us examine how the presence of the channel junction and

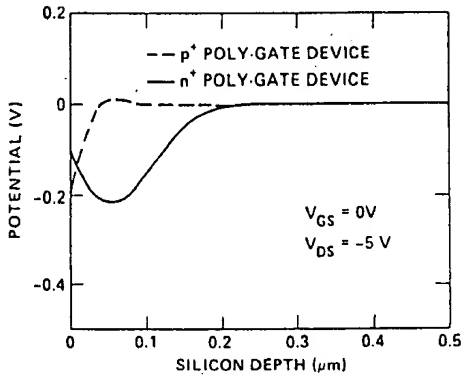

Fig. 5-55 Simulations of the electrical potential perpendicular to the surface in the channel region of two long-channel PMOS devices using GEMINI and SUPREM III simulations of devices with n^+ polysilicon and p^+ polysilicon gates with effective gate lengths of 20 μm.[114] (© 1985 IEEE).